ouput x

input bits {0,1}

12
Convolutional
encoder 1

output y

11
Interleaver

13
Convolutional
encoder 2

output z

Figure 1 Basic Architecture of Turbo Encoder (Coding Rate == 1/3)

x   z

21
MAP
decoder 1

22
Interleaver

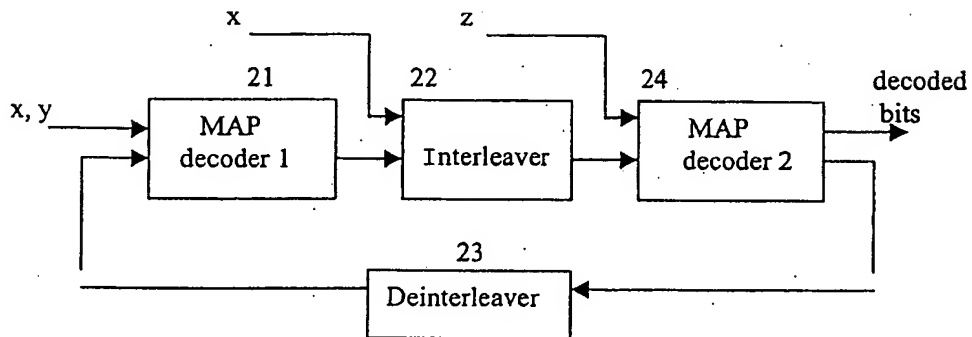24
MAP
decoder 2

decoded
bits

x, y

23
Deinterleaver

Figure 2 Basic Architecture of Turbo Decoder (Coding Rate == 1/3)
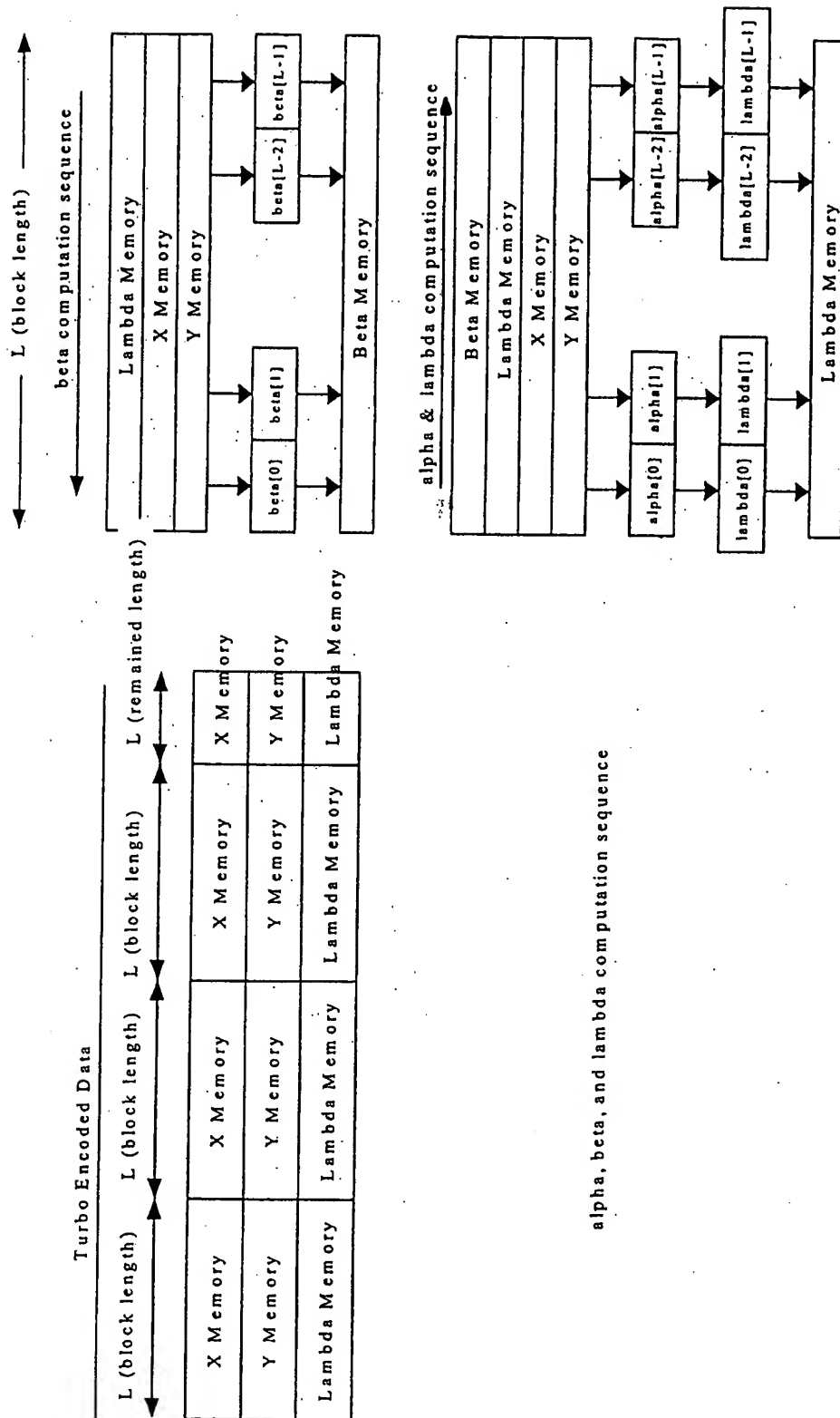
Figure 3.   Alpha, Beta and Lambda Calculation Sequence

State Transition in Beta Computation

State m	0	1	2	3	4	5	6	7
Next[m][0]	0	4	5	1	2	6	7	3
Next[m][1]	4	0	1	5	6	2	3	7

State Transition in Alpha Computation

State m	0	1	2	3	4	5	6	7
prev[m][0]	0	3	4	7	1	2	5	6
prev[m][1]	1	2	5	6	0	3	4	7

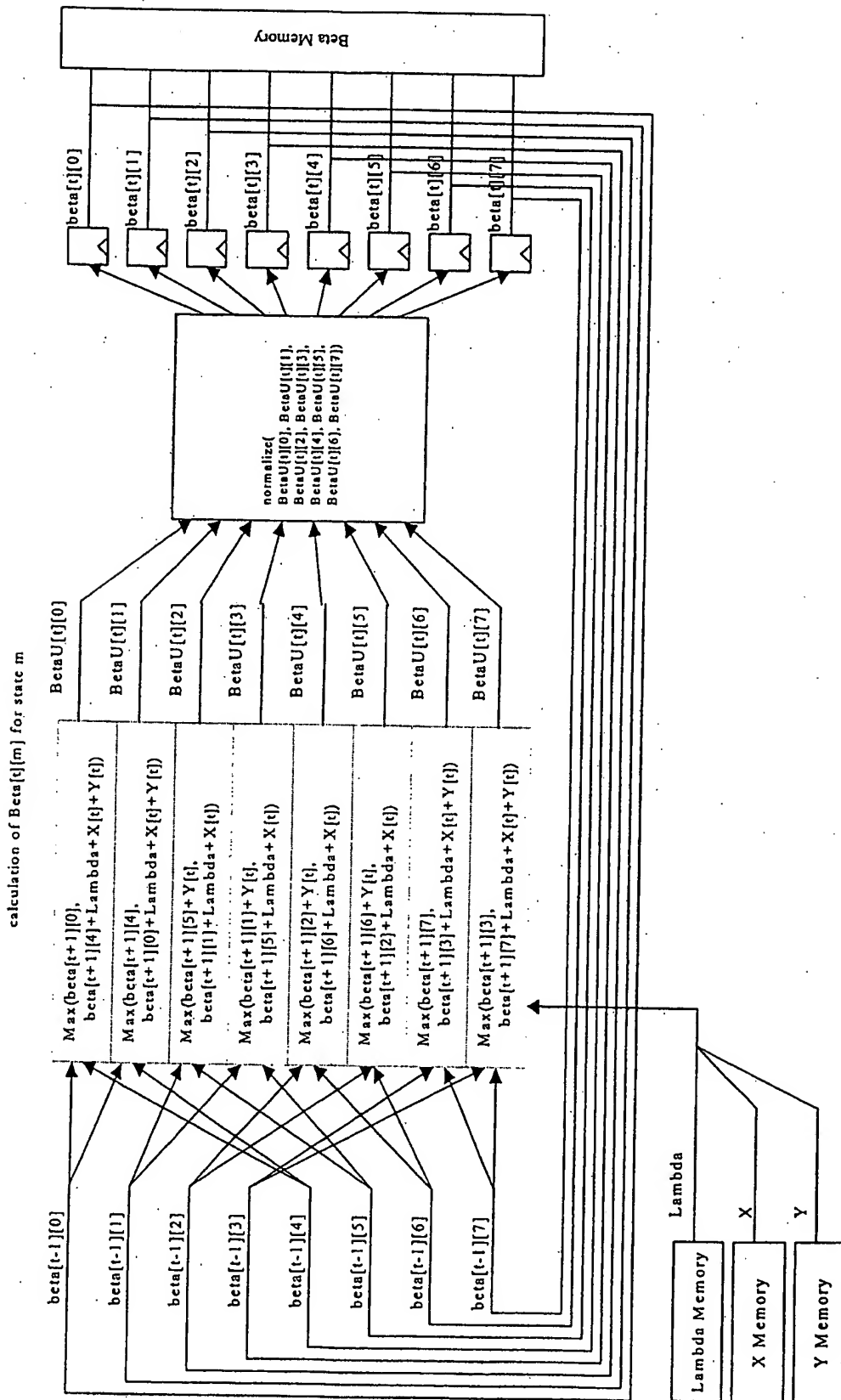Figure 4 State Transition in Beta and Alpha Computation.

Figure 5. Beta Computation Block Diagram

Prior Art

Prior Art
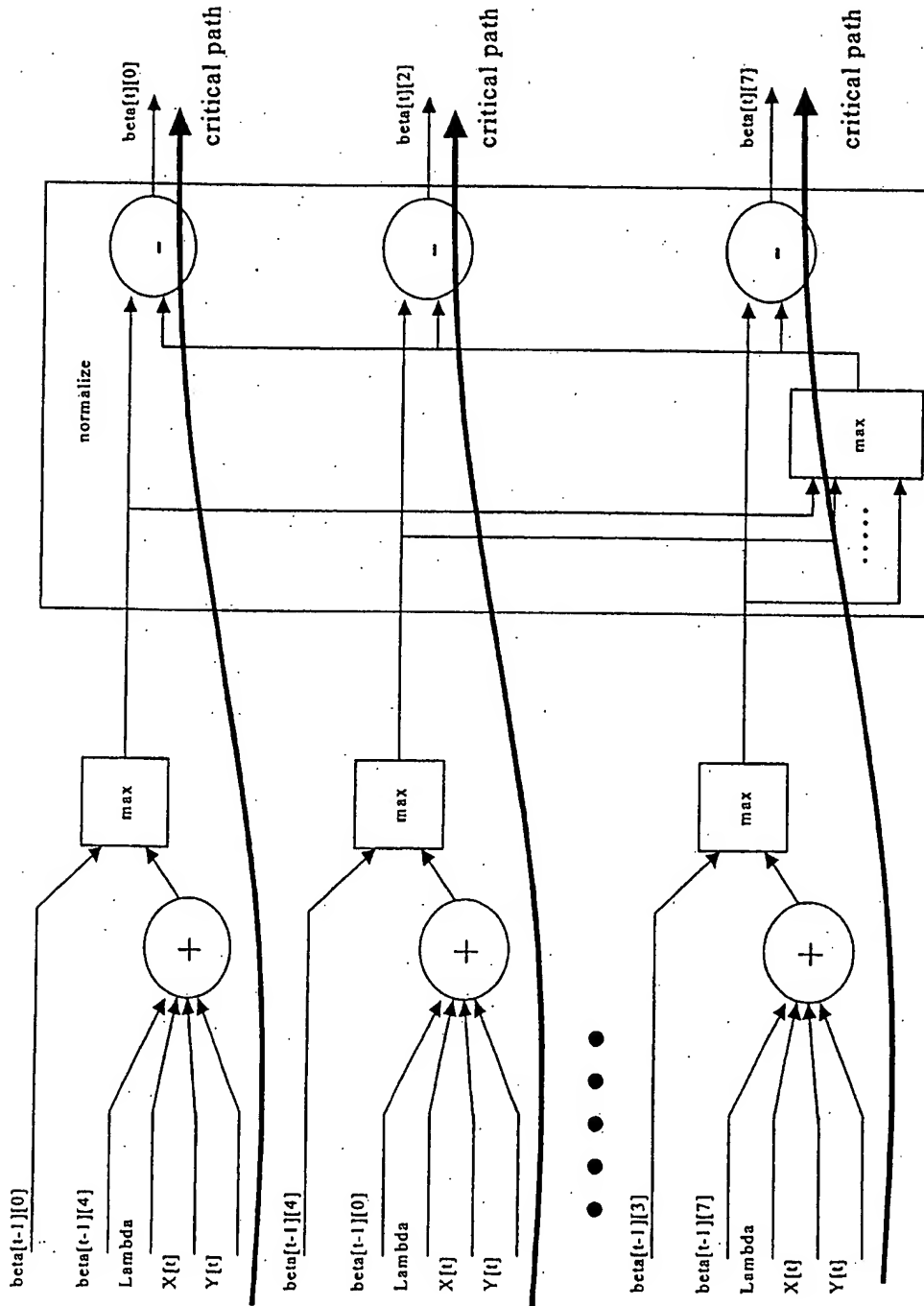
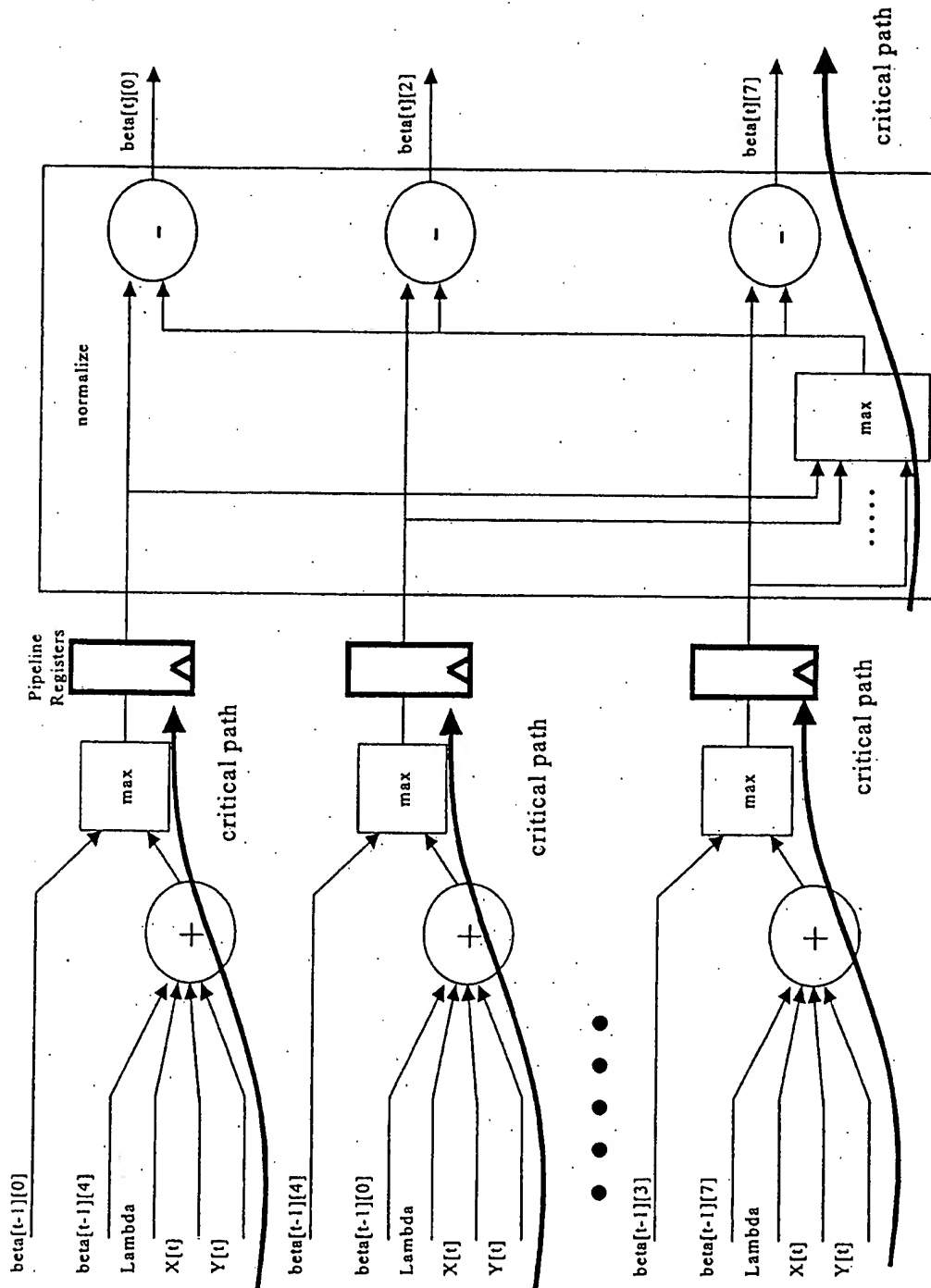Figure 6 Details Beta Computation and Critical Path Block Diagram

Figure 7: The Improved Structure of Beta Computation and Critical Path Diagram
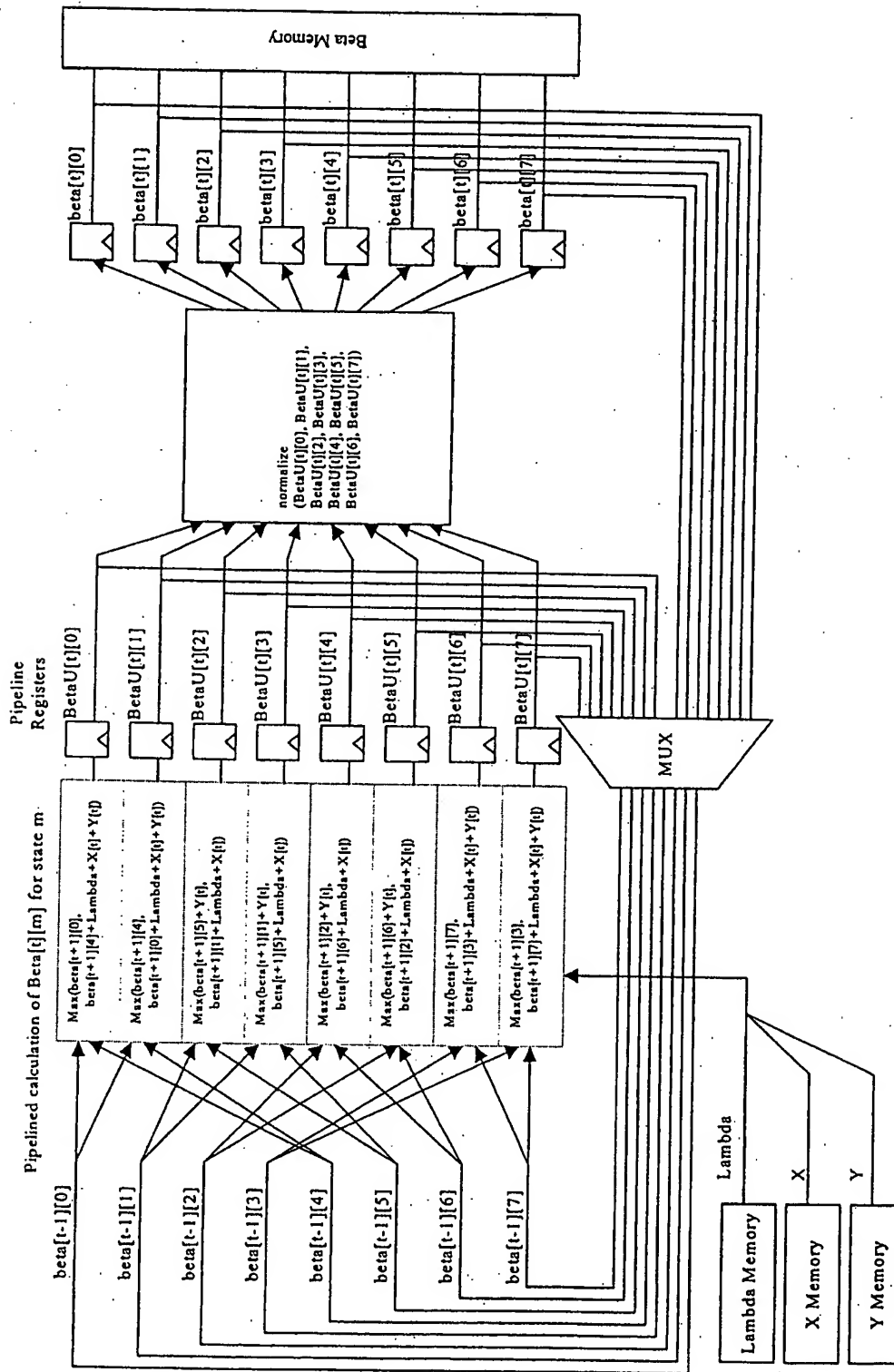
Figure 8 Overall Structure of Pipelined Beta Computation Path Diagram

Beta Computation Stages before pipelining

Beta Computation Stages after pipelining
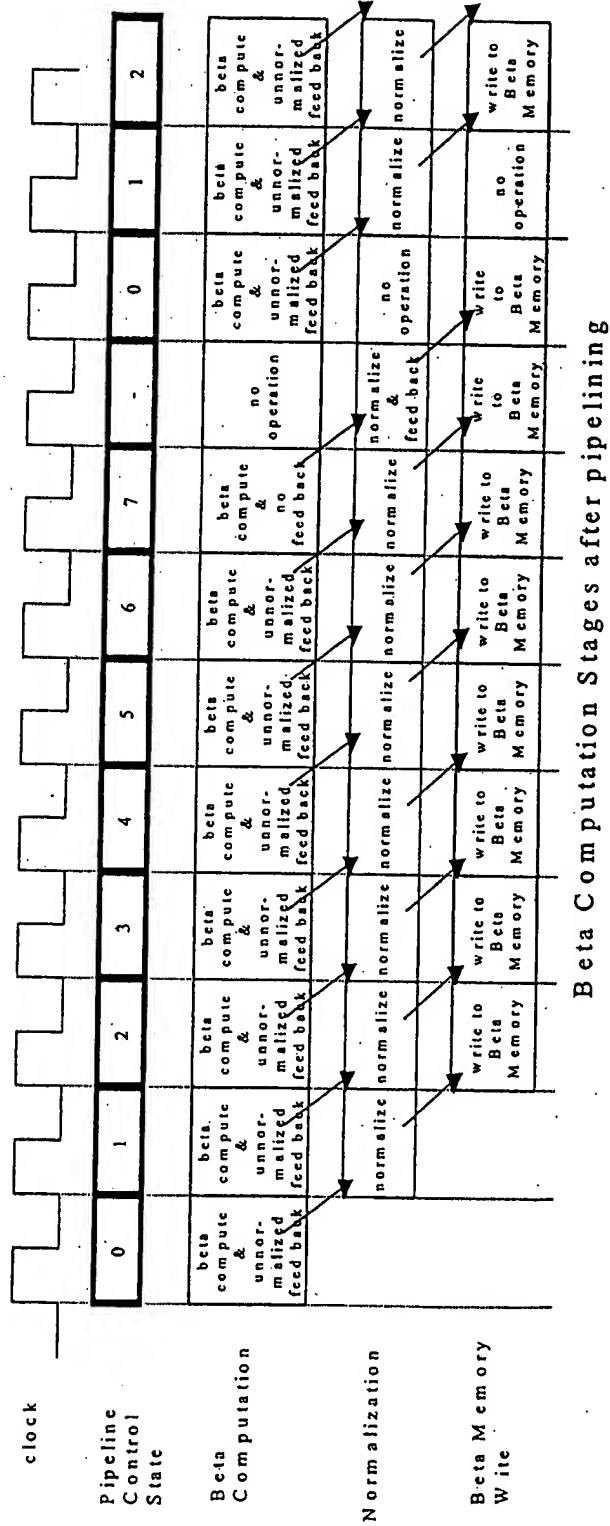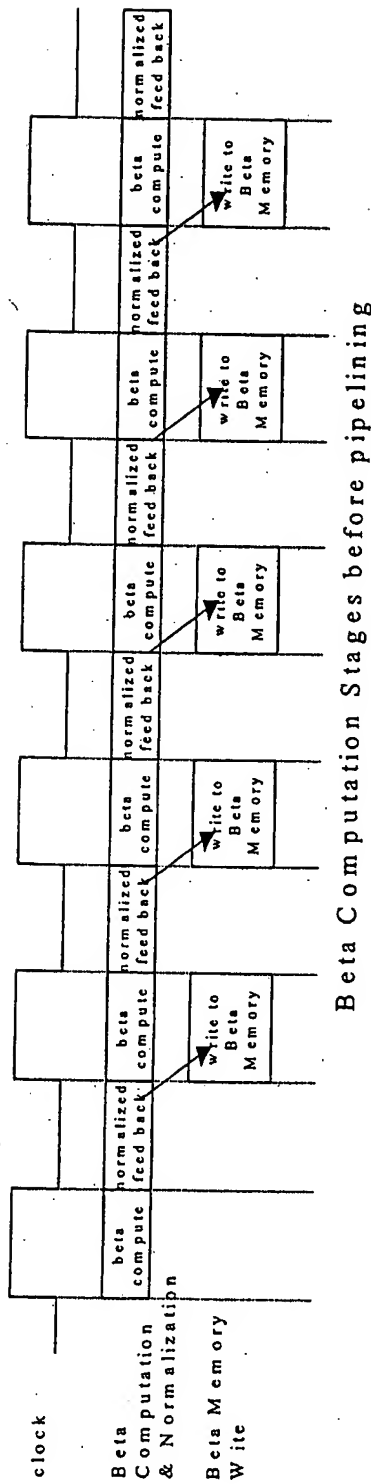
Figure 9 The pipeline Stages of Beta Computation Diagram

calculation of Alpha[t][m] for state m

AlphaU[t][0]
AlphaU[t][1]
AlphaU[t][2]
AlphaU[t][3]
AlphaU[t][4]
AlphaU[t][5]
AlphaU[t][6]
AlphaU[t][7]

normalize
(AlphaU[t][0], AlphaU[t][1],
AlphaU[t][2], AlphaU[t][3],
AlphaU[t][4], AlphaU[t][5],
AlphaU[t][6], AlphaU[t][7])

alpha[t][0]
alpha[t][1]
alpha[t][2]
alpha[t][3]
alpha[t][4]
alpha[t][5]
alpha[t][6]
alpha[t][7]

Max(alpha[t-1][0],
alpha[t-1][1]+Lambda+X[t]+Y[t])

Max(alpha[t-1][3]+Y[t],
alpha[t-1][2]+Lambda+X[t])

Max(alpha[t-1][4]+Y[t],
alpha[t-1][5]+Lambda+X[t])

Max(alpha[t-1][7],
alpha[t-1][6]+Lambda+X[t] +Y[t])

Max(alpha[t-1][1],
alpha[t-1][0]+Lambda+X[t]+Y[t])

Max(alpha[t-1][2]+Y[t],
alpha[t-1][3]+Lambda+X[t])

Max(alpha[t-1][5]+Y[t],
alpha[t-1][4]+Lambda+X[t])

Max(alpha[t-1][6],
alpha[t-1][7]+Lambda+X[t]+Y[t])

alpha[t-1][0]
alpha[t-1][1]
alpha[t-1][2]
alpha[t-1][3]
alpha[t-1][4]
alpha[t-1][5]
alpha[t-1][6]
alpha[t-1][7]

Lambda
X
Y

Lambda Memory
X Memory
Y Memory

Prior Art

Figure 10 Alpha Computation Block Digram

soft output

Lambda Memory

LLR computation

L1

L0

max

max

calculation of Alpha[t][m] for state m

calculation of Lambda[t][m] for state m

alpha1[t][0] + beta[4]
alpha1[t][1] + beta[0]
alpha1[t][2] + beta[1]
alpha1[t][3] + beta[5]
alpha1[t][4] + beta[6]
alpha1[t][5] + beta[2]
alpha1[t][6] + beta[3]
alpha1[t][7] + beta[7]

alpha0[t][0] + beta[0]
alpha0[t][1] + beta[4]
alpha0[t][2] + beta[5]
alpha0[t][3] + beta[1]
alpha0[t][4] + beta[2]
alpha0[t][5] + beta[6]
alpha0[t][6] + beta[7]
alpha0[t][7] + beta[3]

alpha[t-1][0]
alpha[t-1][3]+Y[t]
alpha[t-1][4]+Y[t]
alpha[t-1][7]
alpha[t-1][1]
alpha[t-1][2]+Y[t]
alpha[t-1][5]+Y[t]
alpha[t-1][6]

alpha[t-1][1] + Lambda+X[t]+Y[t]
alpha[t-1][2] + Lambda+X[t]
alpha[t-1][5] + Lambda+X[t]
alpha[t-1][6] + Lambda+X[t] +Y[t]
alpha[t-1][0] + Lambda+X[t]
alpha[t-1][3] + Lambda+X[t]
alpha[t-1][4] + Lambda+X[t]+Y[t]
alpha[t-1][7] + Lambda+X[t]+Y[t]

Beta Memory

alpha[t-1][0]
alpha[t-1][1]
alpha[t-1][2]
alpha[t-1][3]
alpha[t-1][4]
alpha[t-1][5]
alpha[t-1][6]
alpha[t-1][7]

Lambda

X

Y

Lambda Memory

X Memory

Y Memory

Prior Art

Figure 11 Lambda Computation Block Diagram

Figure 12 Details Alpha and Lambda Computation and Critical Path Block Diagram

Prior Art

Figure 13 Improved Structure of Alpha and Lambda Computation and Critical Path Diagram

Figure 14 The Overall Structure of Pipelined Alpha Computation Path Diagram
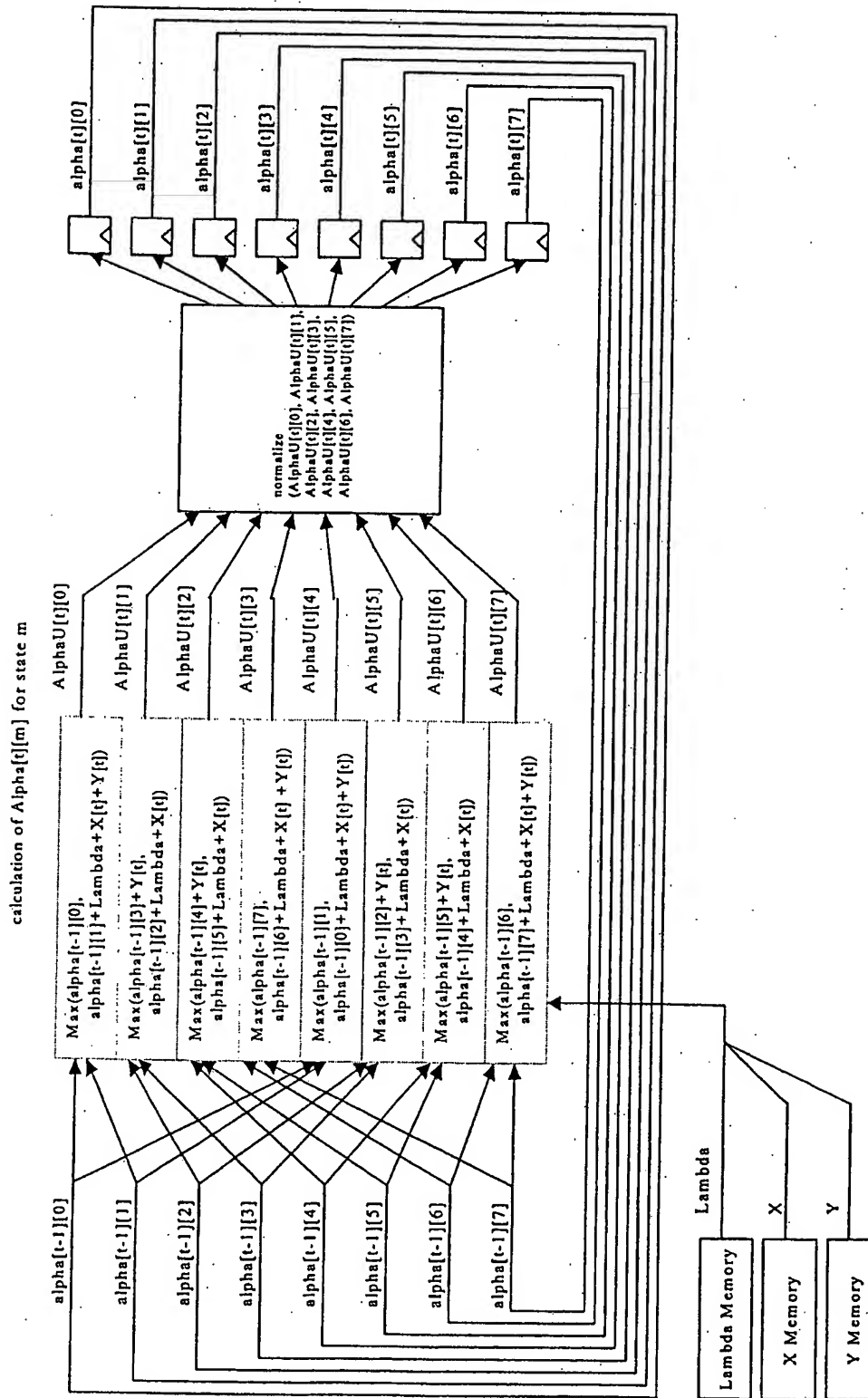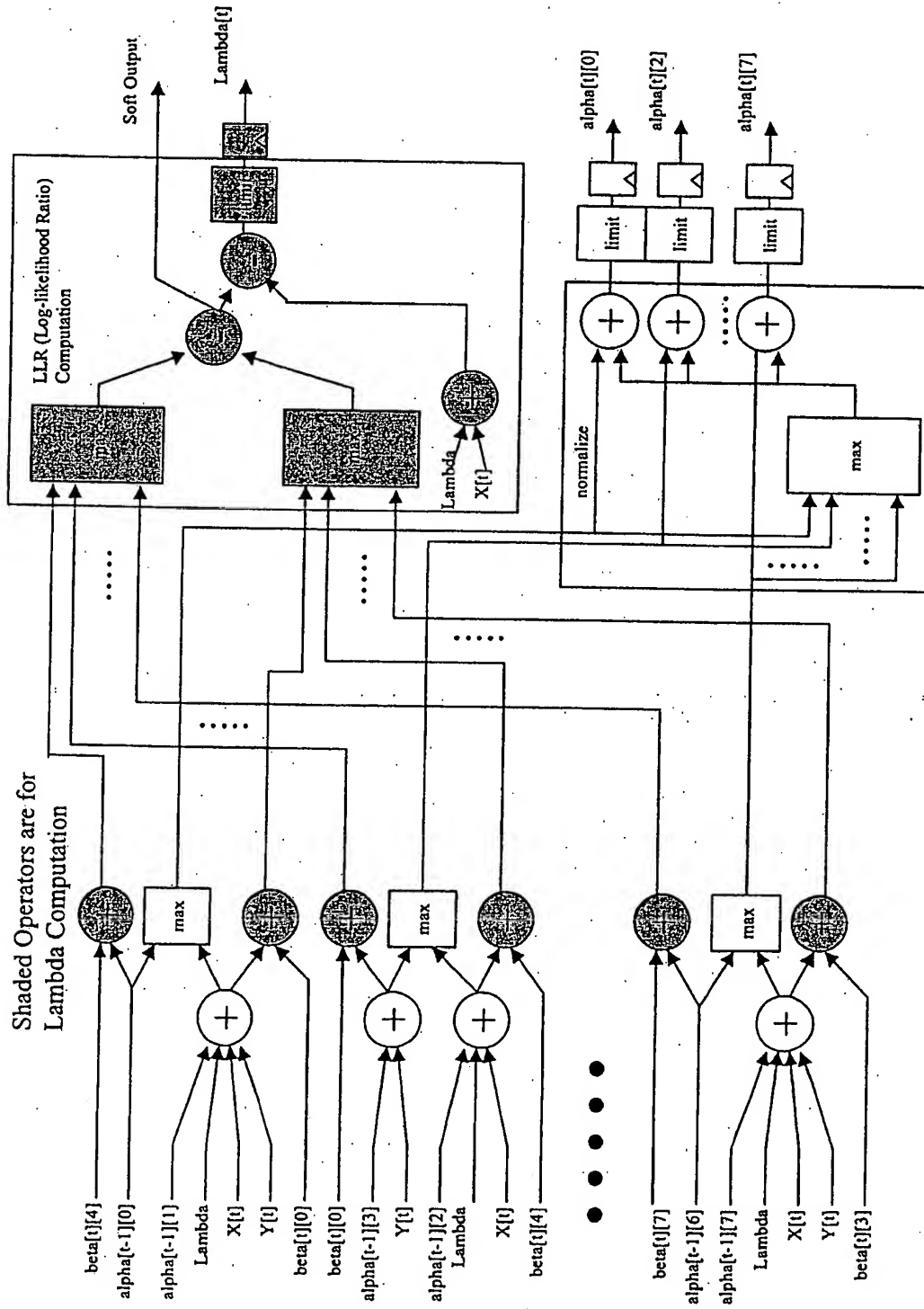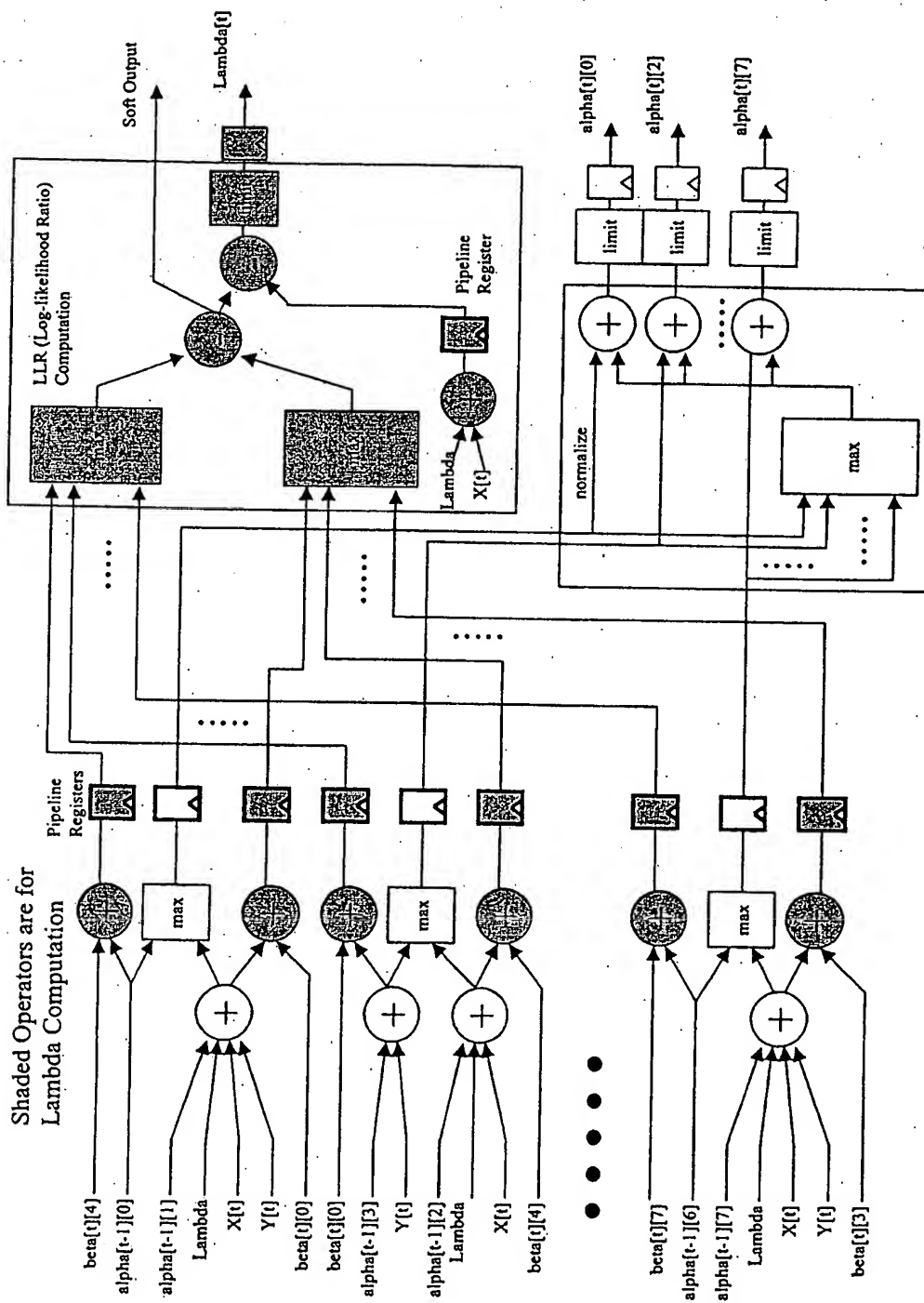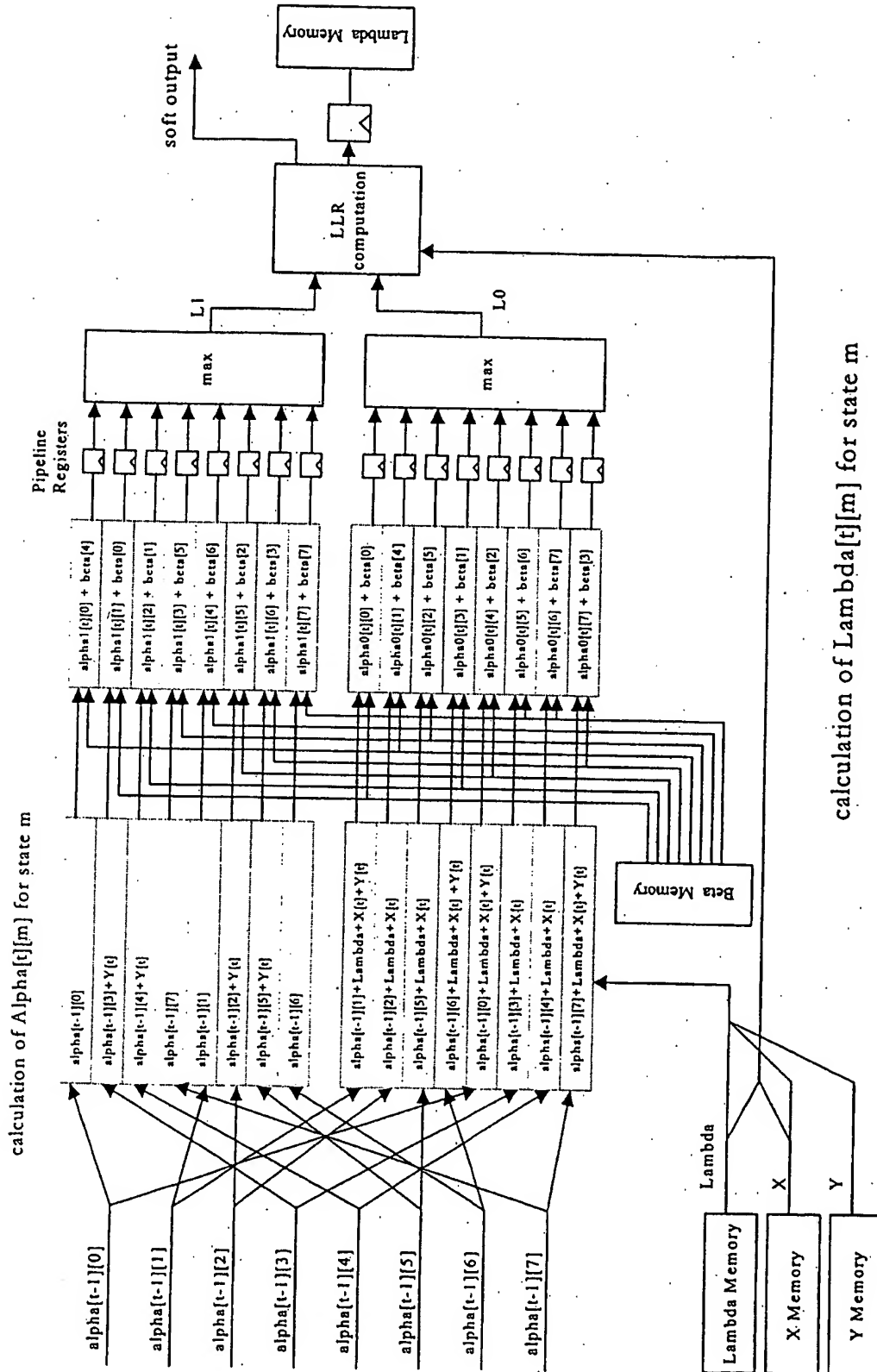
soft output

Lambda Memory

LLR computation

max   L1

max   L0

Pipeline Registers

alpha1[t][0] + beta[4]
alpha1[t][1] + beta[0]
alpha1[t][2] + beta[1]
alpha1[t][3] + beta[5]
alpha1[t][4] + beta[6]
alpha1[t][5] + beta[2]
alpha1[t][6] + beta[3]
alpha1[t][7] + beta[7]

alpha0[t][0] + beta[0]
alpha0[t][1] + beta[4]
alpha0[t][2] + beta[5]
alpha0[t][3] + beta[1]
alpha0[t][4] + beta[2]
alpha0[t][5] + beta[6]
alpha0[t][6] + beta[7]
alpha0[t][7] + beta[3]

calculation of Alpha[t][m] for state m

calculation of Lambda[t][m] for state m

alpha[t-1][0]
alpha[t-1][3]+Y[t]
alpha[t-1][4]+Y[t]
alpha[t-1][7]
alpha[t-1][1]
alpha[t-1][2]+Y[t]
alpha[t-1][5]+Y[t]
alpha[t][6]

alpha[t-1][1]+Lambda+X[t]+Y[t]
alpha[t-1][2]+Lambda+X[t]
alpha[t-1][5]+Lambda+X[t]
alpha[t-1][6]+Lambda+X[t]+Y[t]
alpha[t-1][0]+Lambda+X[t]+Y[t]
alpha[t-1][3]+Lambda+X[t]
alpha[t-1][4]+Lambda+X[t]
alpha[t-1][7]+Lambda+X[t]+Y[t]

Beta Memory

alpha[t-1][0]
alpha[t-1][1]
alpha[t-1][2]
alpha[t-1][3]
alpha[t-1][4]
alpha[t-1][5]
alpha[t-1][6]
alpha[t-1][7]

Lambda

Lambda Memory

X

X Memory

Y

Y Memory

Figure 15 The Overall Structure of Pipelined Lambda Computation Path Diagram
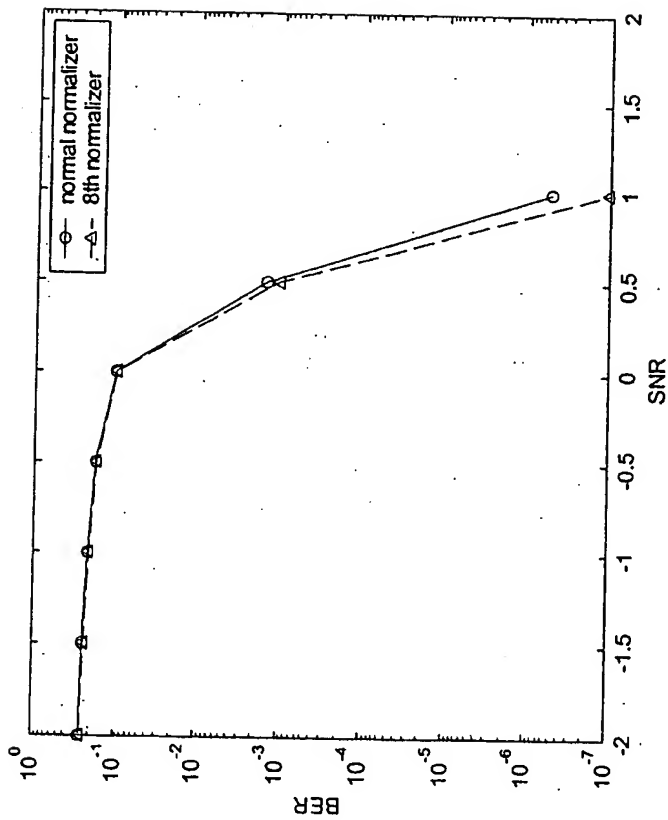
Figure 16 BER and SNR simulation for original normalization and new normalization
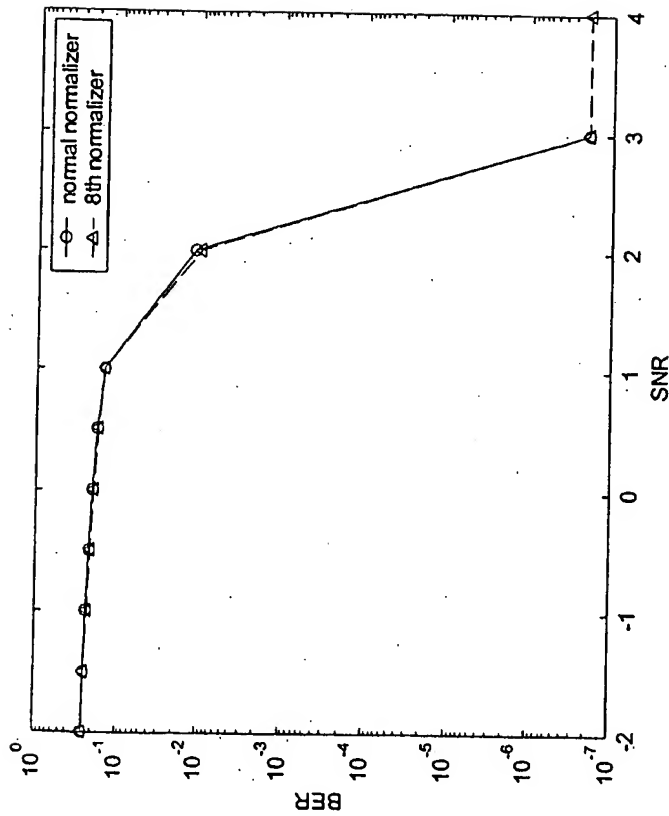Block length = 3856 bits)

Figure 17 BER and SNR simulation for original normalization and new normalization
(Block length = 5114 bits)